Welcome to Tech Tuesday

by Vic Myers Associates

PRESENTED IN PARTNERSHIP WITH

Acromag
THE LEADER IN INDUSTRIAL I/O

PRESENTER TODAY IS GREG VITEL, NATIONAL SALES MANAGER FOR ACROMAG EMBEDDED SOLUTIONS

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FPGA Zynq® UltraScale+™ Agenda

TYPES OF ZYNQ ULTRASCALE+

FEATURES OF ACROPACK ZYNQ ULTRASCALE+

APZU CARRIER BOARDS

DEVELOPMENT TOOLS

EDK AND SOFTWARE

APPLICATIONS

FPGA PRODUCT LINES SUPPORTED

QUESTIONS

Zynq® UltraScale+™ MPSoC Chip

Zynq Chip is the XCZU3CG-2SBVA484I

- The CG has Dual-Core Cortex-A53 (APU)
- Neon (Media Processing Engine)
- Dual-Core Cortex R5 (RPU)

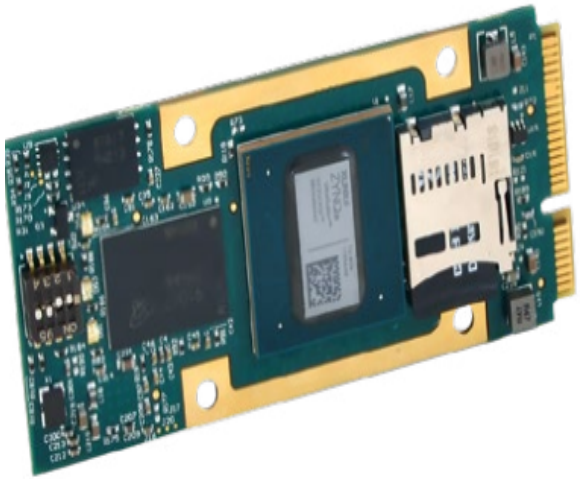
Zynq EG

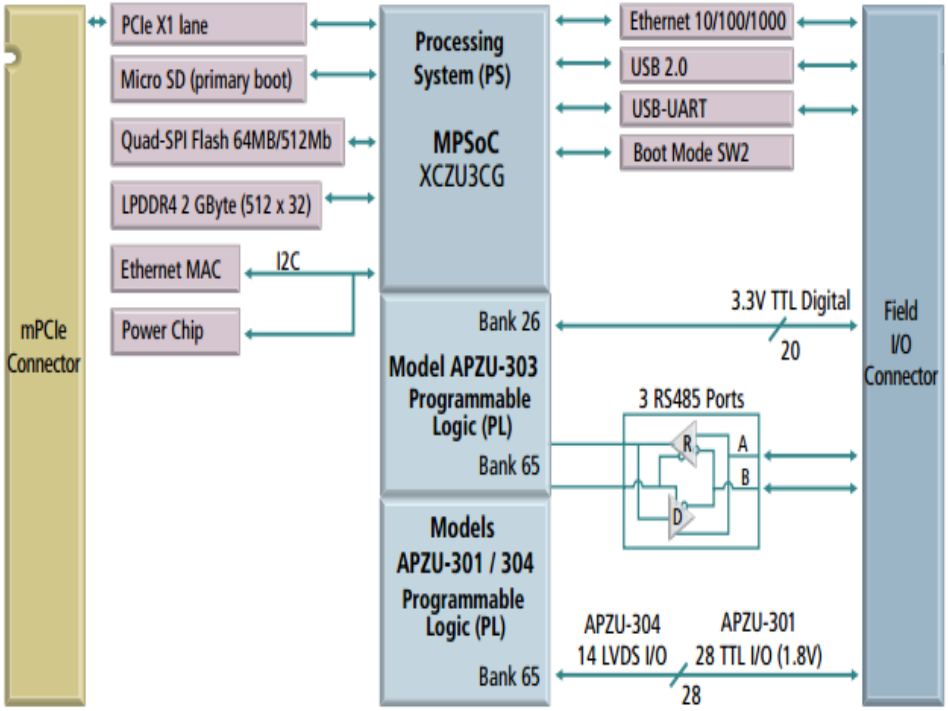
- The EG have Quad-Core Cortex-A53
- Neon (Media Processing Engine)
- Dual-Core Cortex R5
- Includes Graphics Processing Unit (Mali-400MP2)

Zynq EV

- The EV have Quad-Core Cortex-A53
- Neon (Media Processing Engine)
- Dual-Core Cortex R5
- Includes Graphics Processing Unit
- Includes Video Codec (H.264/H.265)

APZU-30x with Zynq Ultrascale+ Overview





ZYNQ

Model
APZU-301: 28 TTL channels
APZU-303: 20 TTL and 3 EIA-485/422 channels
APZU-304: 14 LVDS channels
5028-626: APZU Break-Out Panel

Zynq UltraScale+ MPSoC Processors CG

Dual Core ARM Cortex-A53

- Up to 1.3GHz operation
- Harvard architecture
  - 64-bit data
  - 64-bit instruction

Dual Core ARM Cortex R5

- Up to 533 MHz operation
- 32-bit Architecture
- Hardware floating-point Unit

Media-Processing Engine

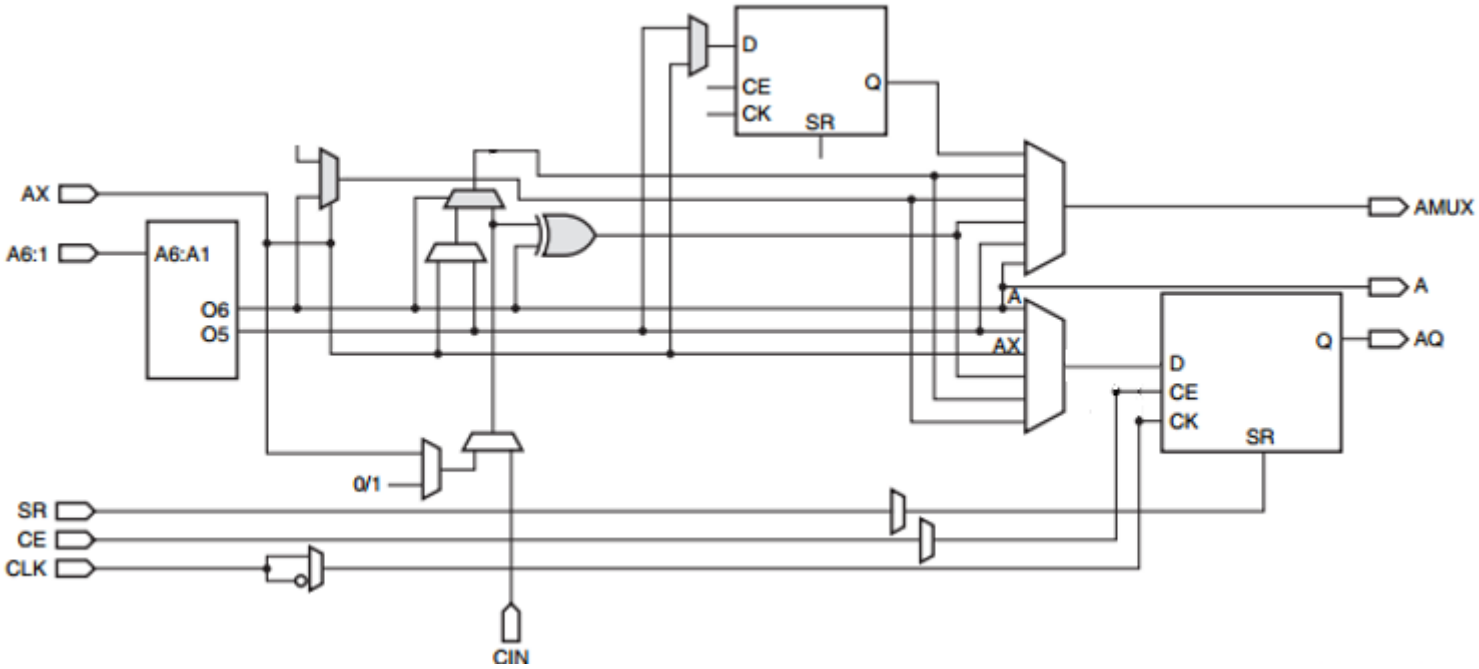
NEON Processor

- Advanced Single Instruction Multiple Data (SIMD) architecture extension for the ARM Cortex-A and Cortex-R series processors
- Accelerates audio and video encoding and decoding
- Accelerates Signal Processing algorithms

FPGA Logic Cell

FPGA (Field Programmable Gate Array)

- 6-input LUT and the Logic Cell




```
process (CK, SR)
begin
    if (SR = '1') then
       AQ <= '0';
    elsif rising_edge(CK) then
       AQ <= ( WriteStb and AXI_d0 and valid) or (AQ and not WriteStb);
    end if;
end process;
```

FPGA Device Capacity

How is device capacity measured?

	XC7A50T	XC7A200T	XC7K325T
Logic Cells	52,160	215,360	326,080
6-input LUT	32,600	134,600	203,800

- Logic Cell = 4 input LUT and 1 Flip Flop
  - 134,600 x 1.6 = 215,360

	ZU3CG
Logic Cells	154,350
6-input LUT	70,560

  - 70,560 x 2.1875 = 154,350

Processor Memory

32KB L1 Caches

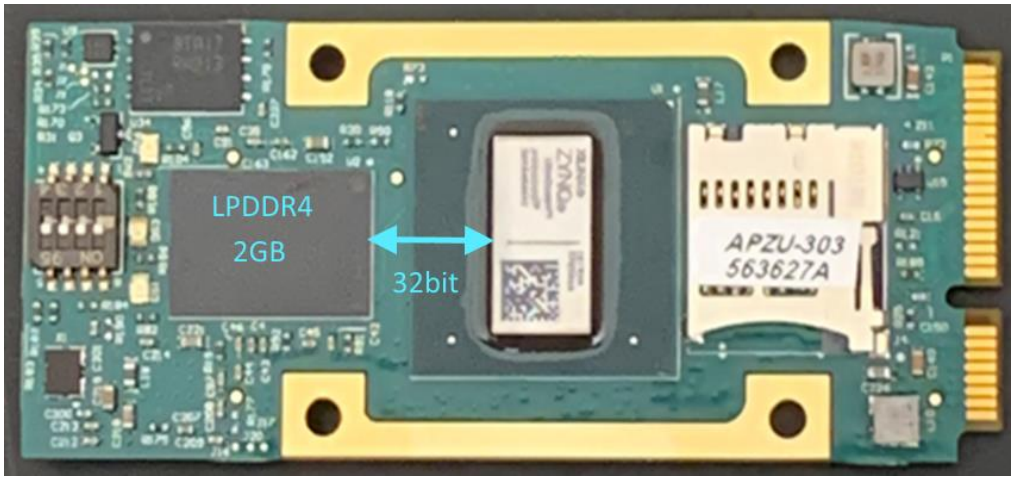
- Fastest but specific to processor

1MB unified L2 Cache

- Faster and shared between processors

2GB LPDDR4 Main Memory

- 32-bit data width

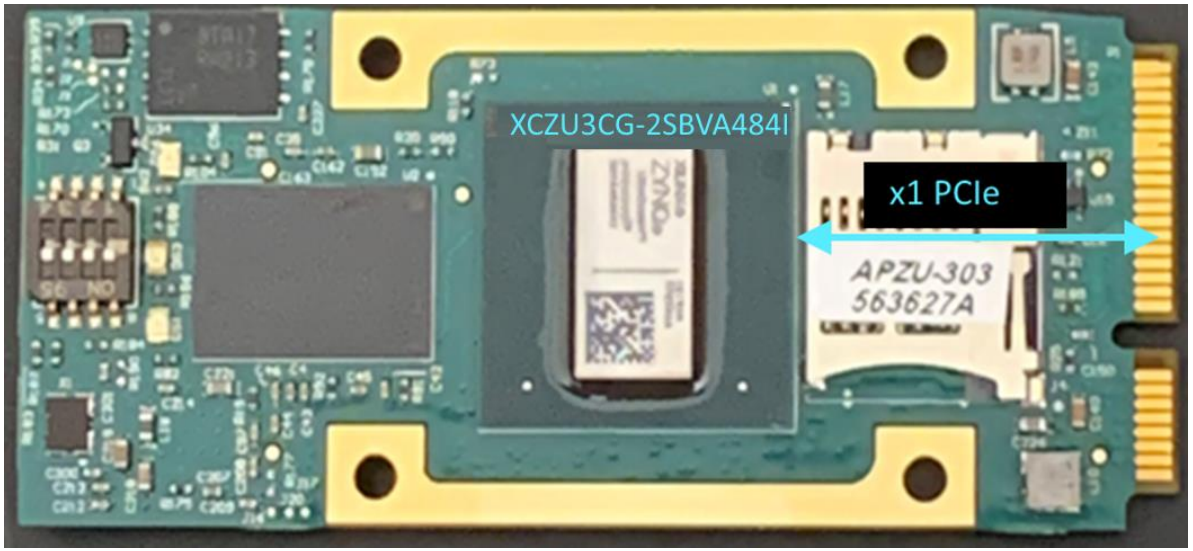


PCIe Interface

APZU include PCIe

- x1 at Gen1 rates
- Compliant PCIe Base Specification Revision 3.1

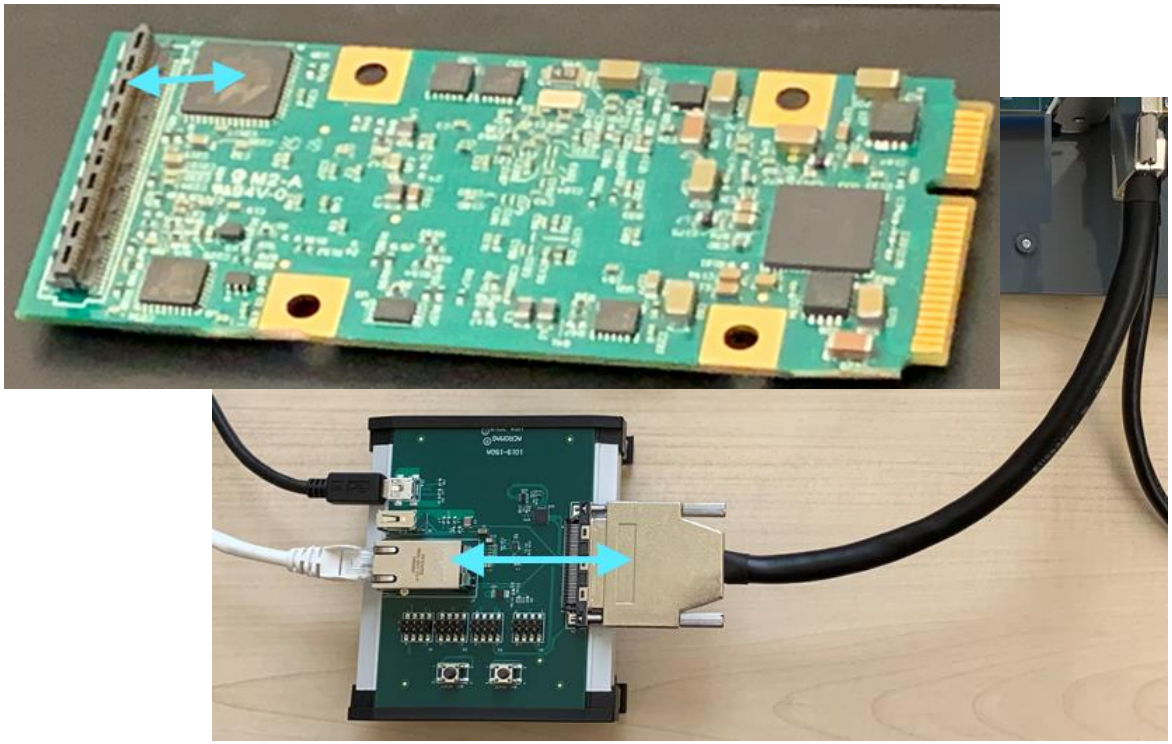
2 general-purpose DMA controllers



APZU I/O Peripherals

Triple-Speed Gigabit Ethernet

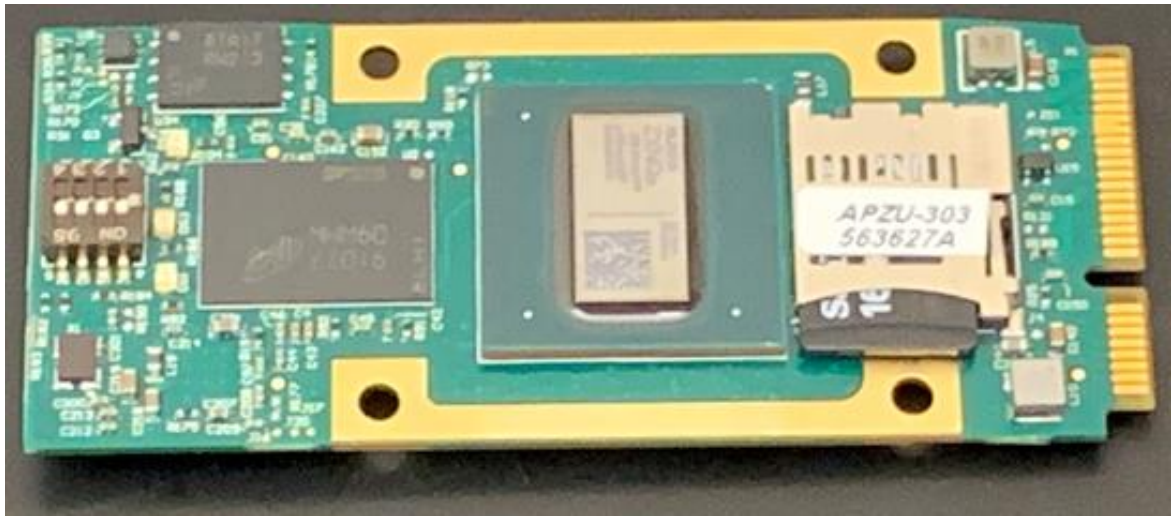
- Compatible with IEEE Std 802.3 and supports 10/100/1000Mb/s transfer rates
  - Reduced Gigabit Media Independent Interface(RGMII)



APZU I/O Peripherals

SD Controller

- Secure digital (SD) interface
- Supports primary boot from Card

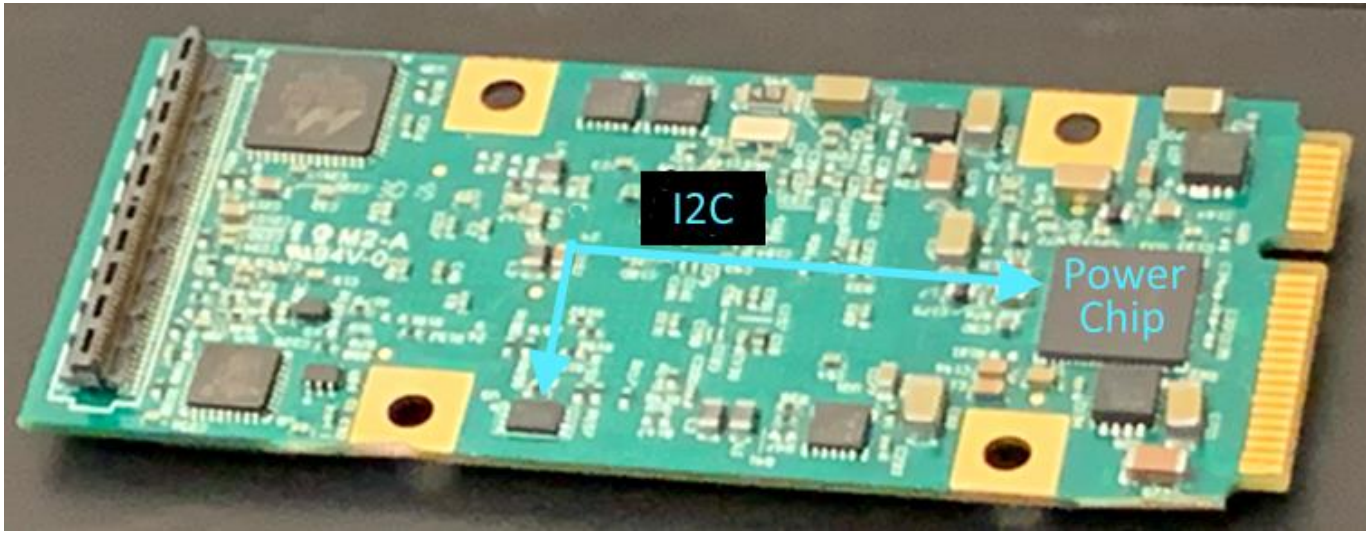


- 16GB microSD Flash Card

APZU I/O Peripherals

I2C

- 2K-bit EEPROM
- Power Chip



SWaP Optimized

Size = 70mm x 30mm
Weight = 35.18 g (including heat spreader)
Power = <5 watts

Actual picture

APZU-30x with included heat spreader

APZU PCIe Carriers

Acropack® Carriers PCIe server slot based

- APCe7012
  - Supports 1 AcroPack
  - Supports Analog Isolated Modules
  - Available in ½ height
  - 68 pin 0.8mm connector
- APCe7022
  - Supports 2 AcroPacks
  - Two 68 pin 0.8mm connector
  - PCIe x4 edge connector
- APCe7040/APCe7043 (3/4 length)
  - Supports 4 AcroPacks
  - Supports Analog Isolated Modules
  - 68 pin 0.8mm connector
  - PCIe x4 edge connector

Other Acropack Carriers for APZU

XMC Acropack Carrier

- XMCAP2020/XMCAP2021/2022
  - Supports 2 AcroPack modules
  - Either front I/O or Rear I/O (P16/P4)
  - Not compatible with conduction cooled carriers
- 6U VPX VPX4520/21
  - Supports 4 AcroPack modules + 1 XMC
  - Supports isolated analog modules
  - Available in front I/O or rear (conduction cooled) versions.

ACEX-4041 Carrier

- Hosts 4 AcroPack modules, M.2 storage and Type 10 Com Express processor

ARCX-1100 packages ACEX-4041 in IP65 chassis with removable 2.5” SSD

Other APZU Carriers

ACPS3310/20 Compact PCIe Serial

- Supports 2 AcroPack Modules
- Supports Isolated Analog
- Either front or rear I/O (to backplane)

EDK and Software Drivers

APZU-EDK (Engineering Design Kit)

- Example of IP block design, block RAM, system monitor, AXI interface to digital I/O

5028-626

- (I/O breakout panel with 68pin cable), M/M, 1 ft.

APSW-API- LNX

- (website download)

APSW-API-WIN

- (DLL Drivers)

APSW-API-VXW

- (VxWorks 7.0)

Development Tools

Vivado® 2020.1 Design Suite

Vitis™

- Unified software platform enables the development of embedded software on Xilinx® platforms including FPGAs, SoCs, and Versal ACAPs.

PetaLinux is an Embedded Linux® Systems Development Kit that targets Xilinx SoC designs

- Includes U-Boot, Linux kernel, Device Tree, and Root Filesystem components.

5028-626 Breakout Board

- The breakout panel and short 68-pin male to male 1’ cable will bring an ethernet port, USB 2.0 port, UART to USB port, digital I/O at jumper blocks, and power and reset buttons out to the field.

Applications for APZU

Protocol converter

Hardware in the loop

Video capture and recording

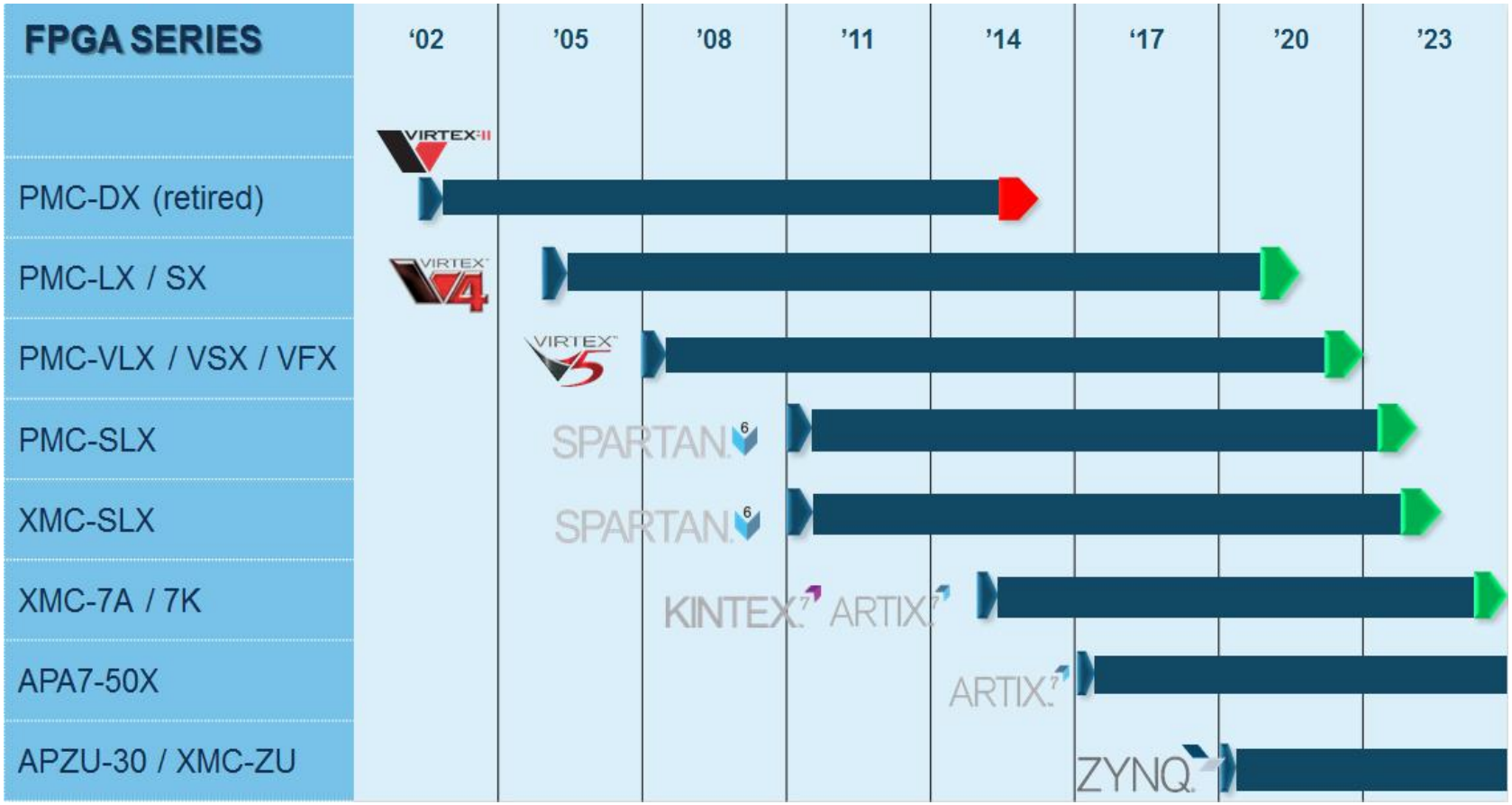
- Cameralink, USB, Ethernet

Video packet interrogation

Missile simulation

Sensor data acquisition

FPGA Product Lines



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