Welcome to Tech Tuesday from Vic Myers Associates

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FPGA Design Modification Walk Through

Tuesday, August 18, 2020

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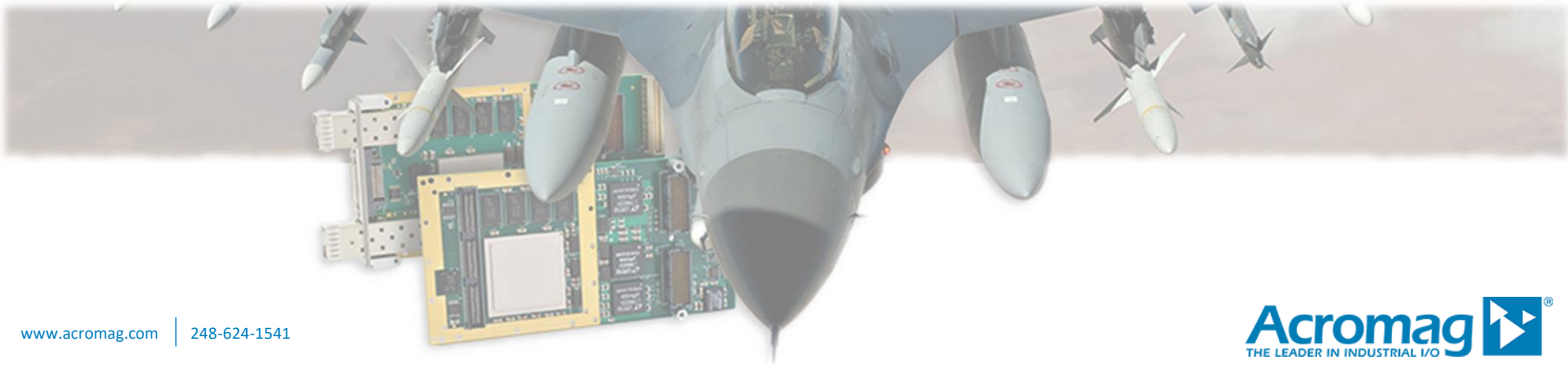
FPGA Design Modification Walk Through

- XMC 7A Block Diagram
- XMC-7A200 Design Mod.
  - Vivado 2019.2
  - Acromag Example Design
- Compile Project
- Produce new MCS file



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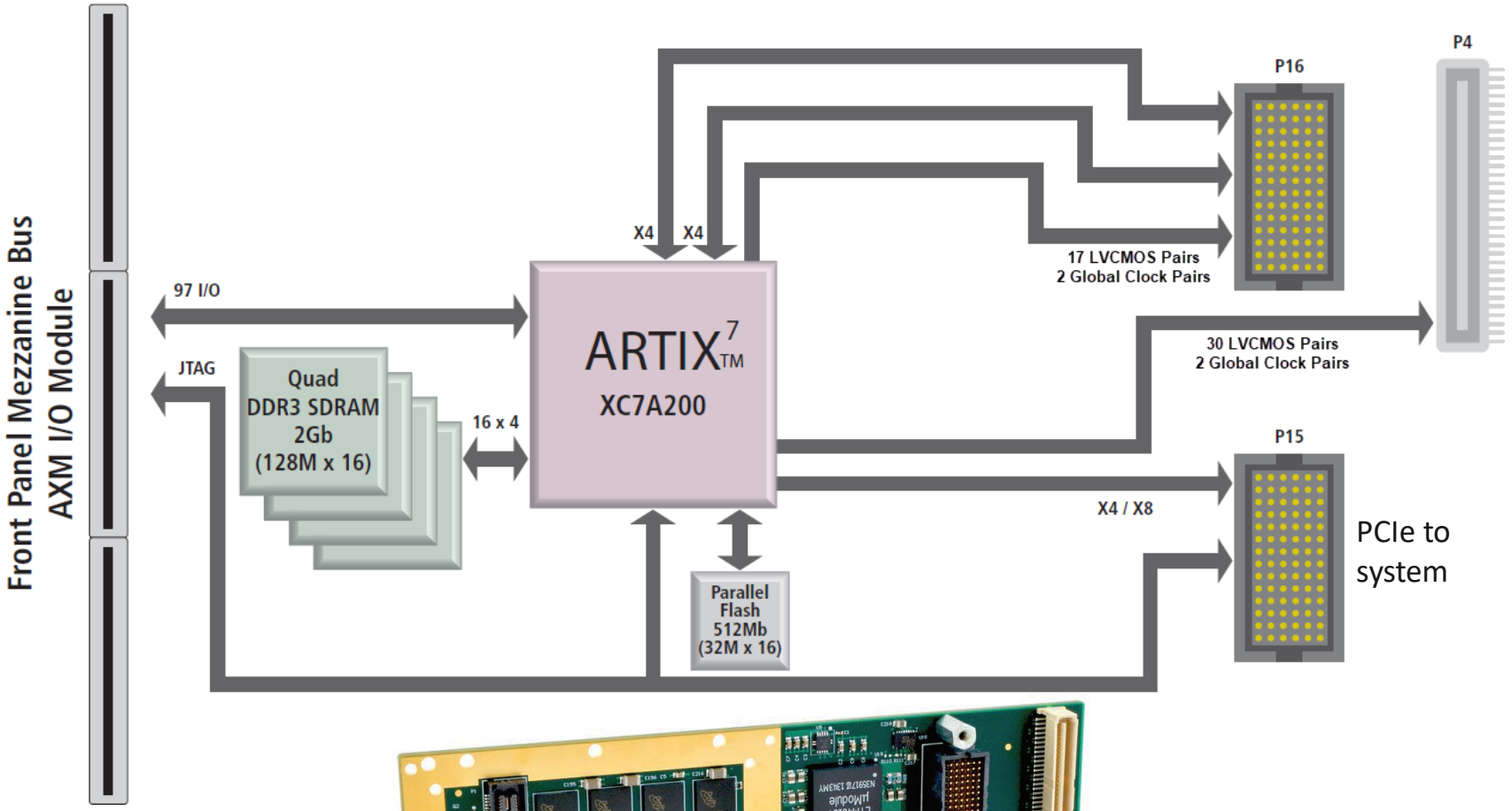
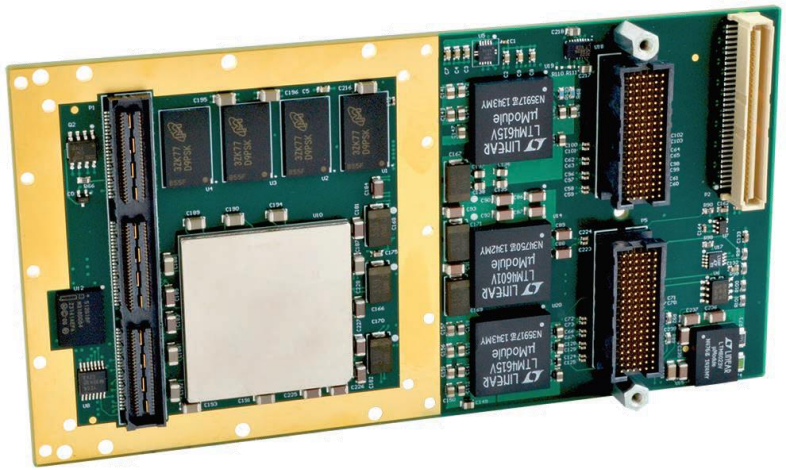
XMC-7A200 Block Diagram





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XMC-7A200 Design Modification Walk Through

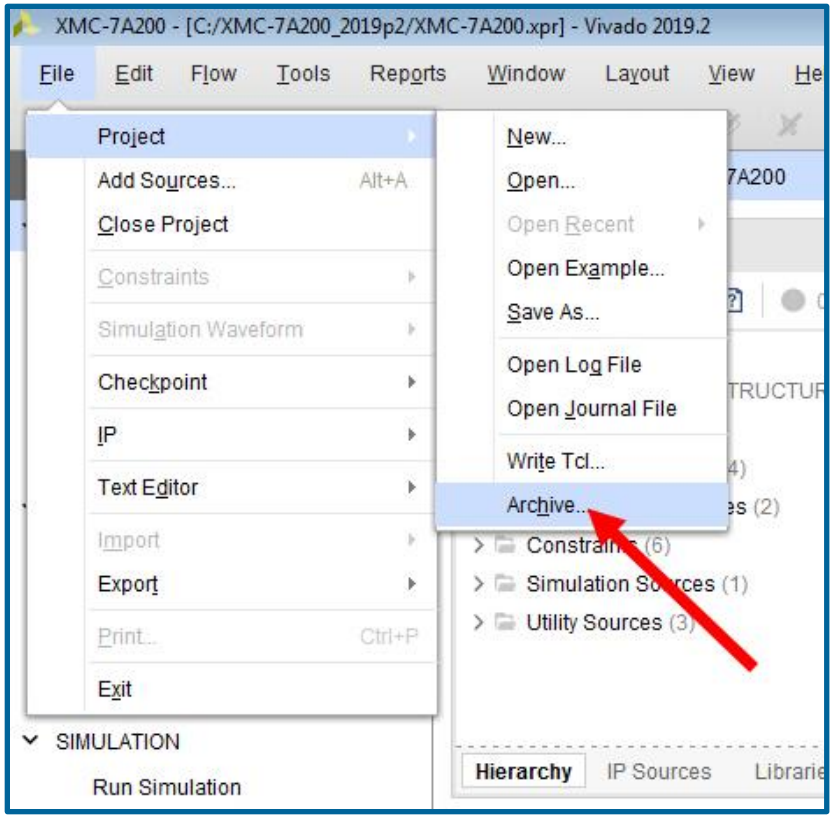
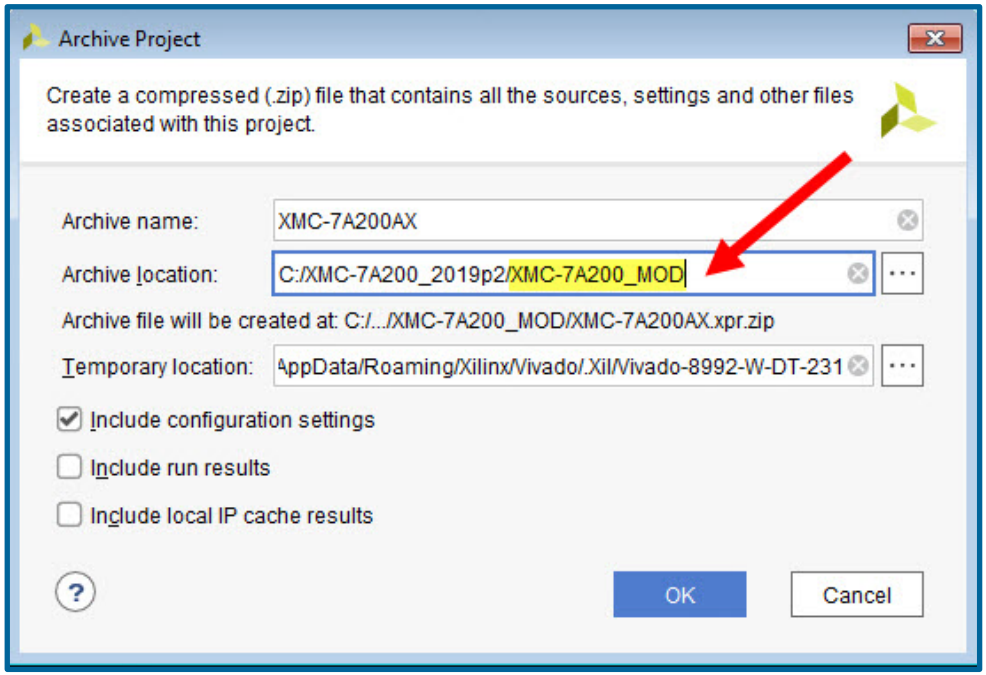


Figure 1

Extracted Archived Project:

C:\XMC-7A200_MOD\XMC-7A200AX.xpr\XMC-7A200\

Figure 2



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XMC-7A200 Design Modification Walk Through

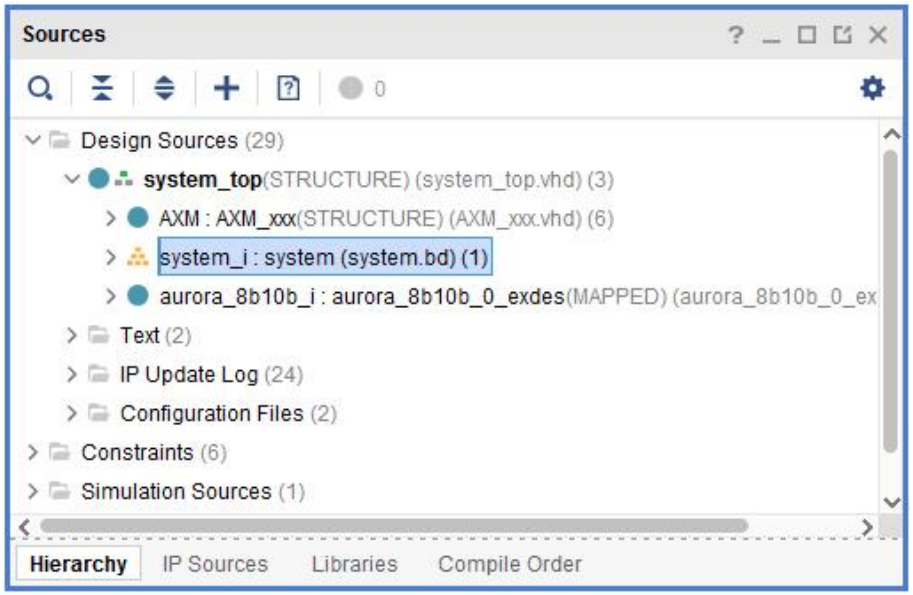
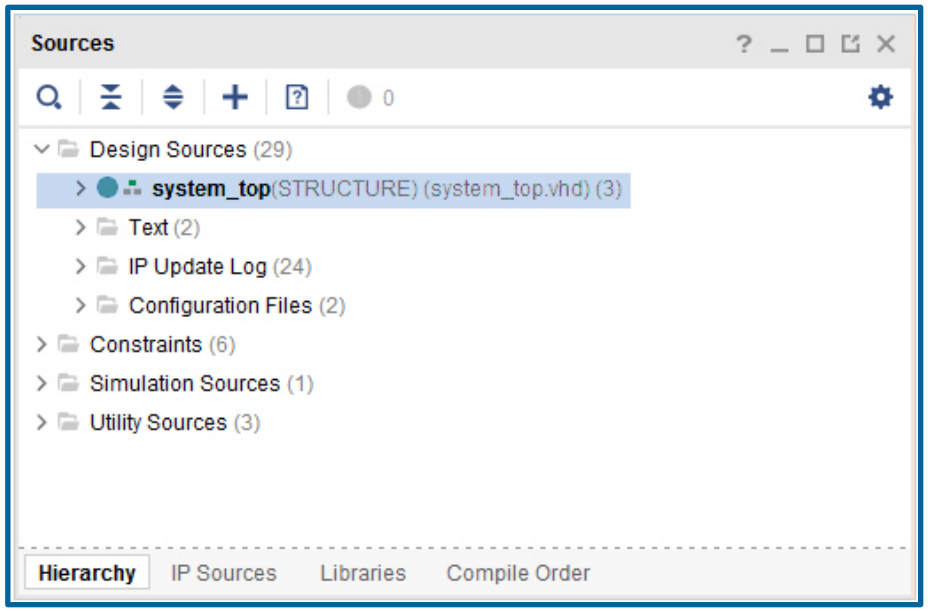


Figure 4

Figure 3



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XMC-7A200 Design Modification Walk Through

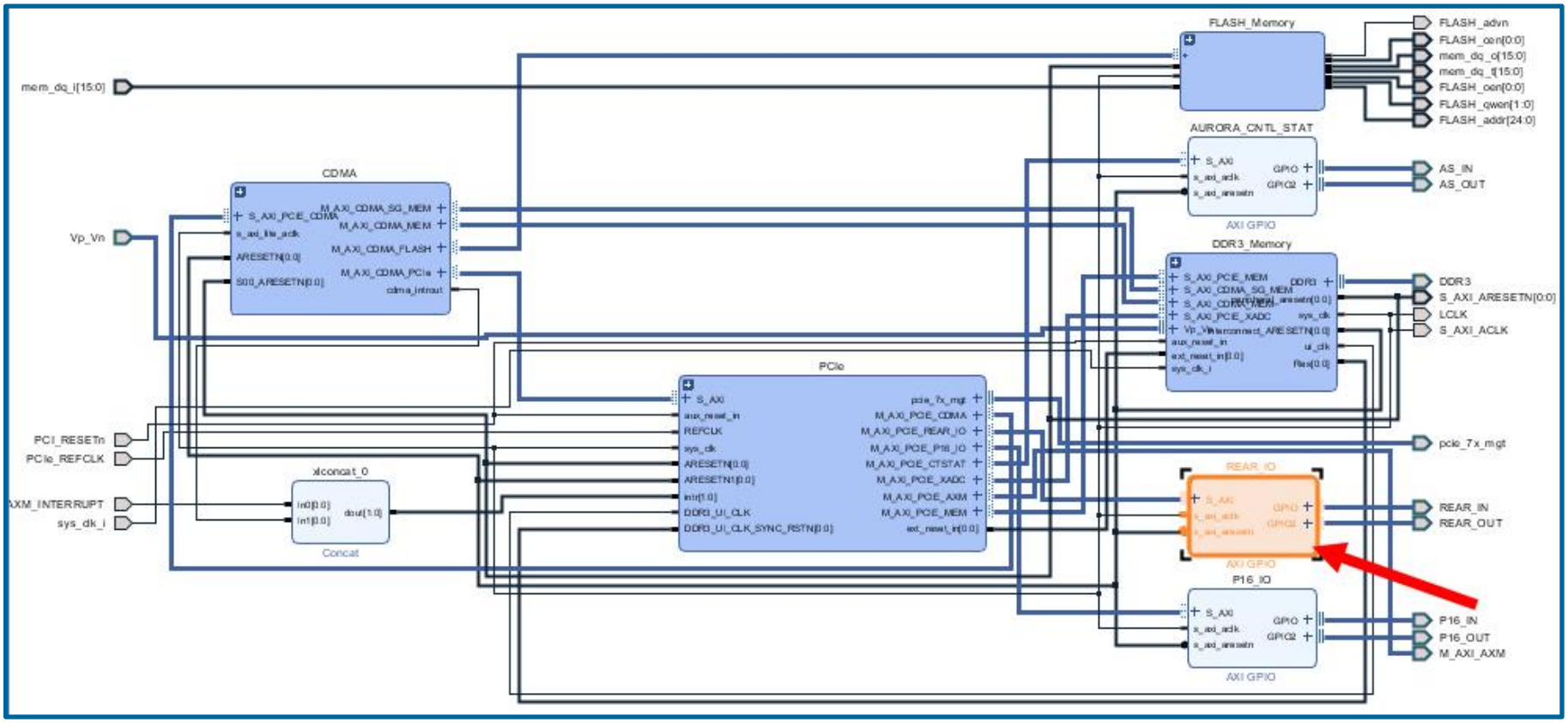


Figure 5

XMC-7A200 Design Modification Walk Through

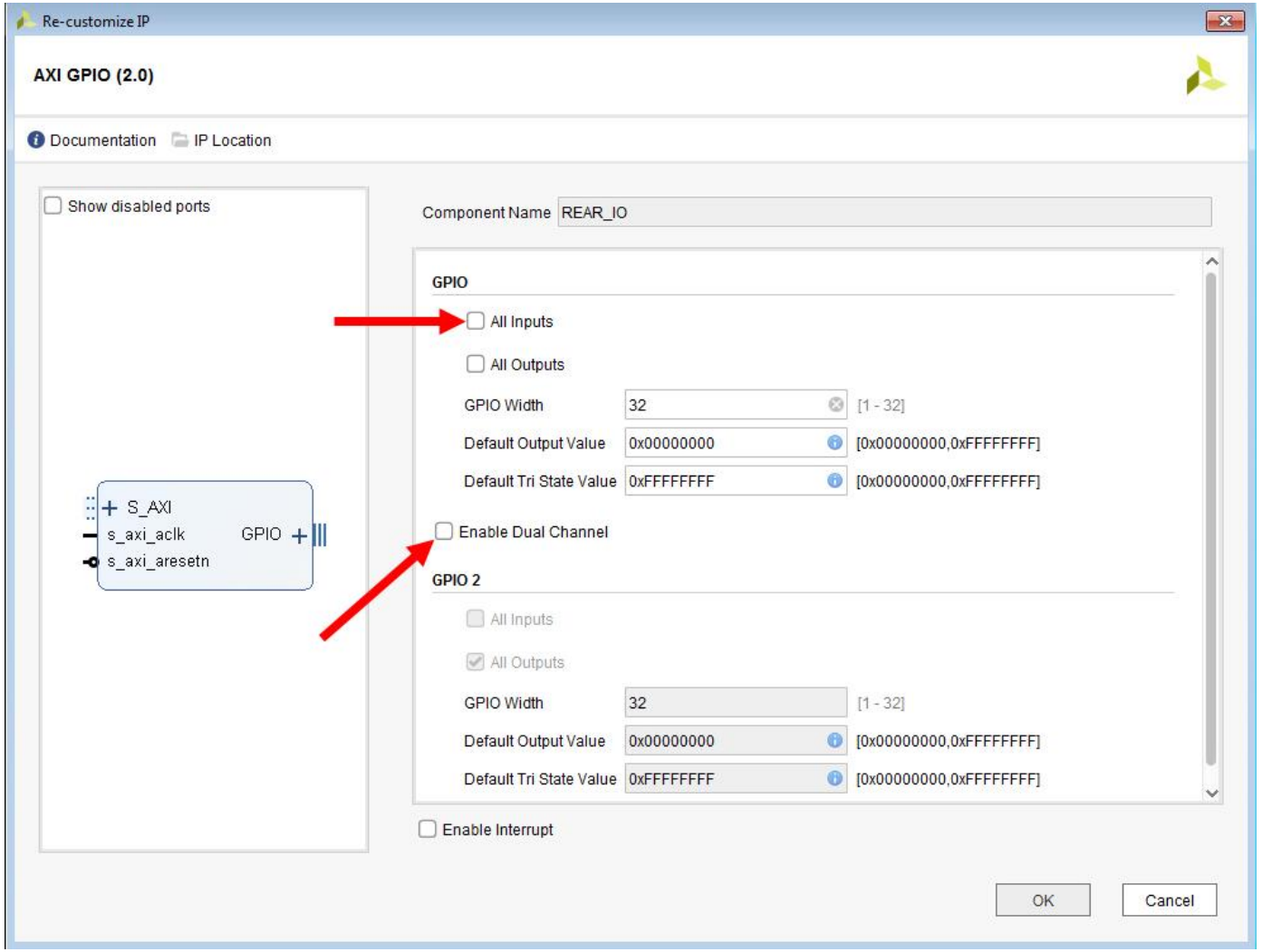
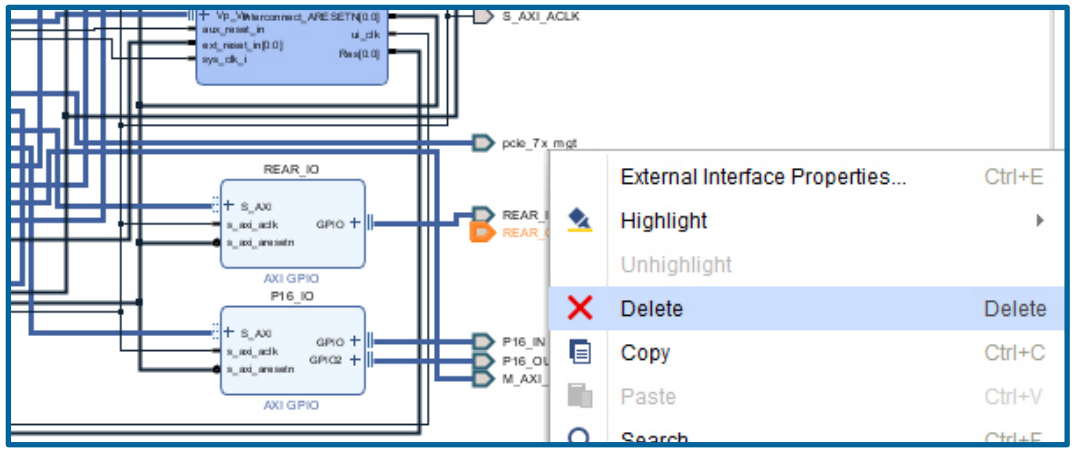


Figure 6

XMC-7A200 Design Modification Walk Through

Figure 7



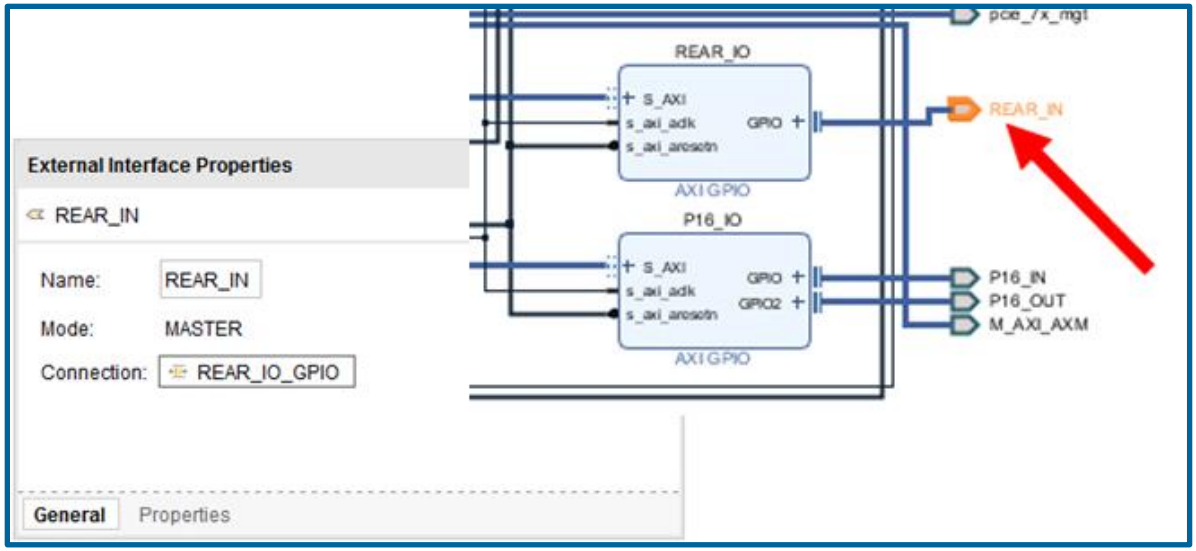


Figure 8

XMC-7A200 Design Modification Walk Through

Figure 9

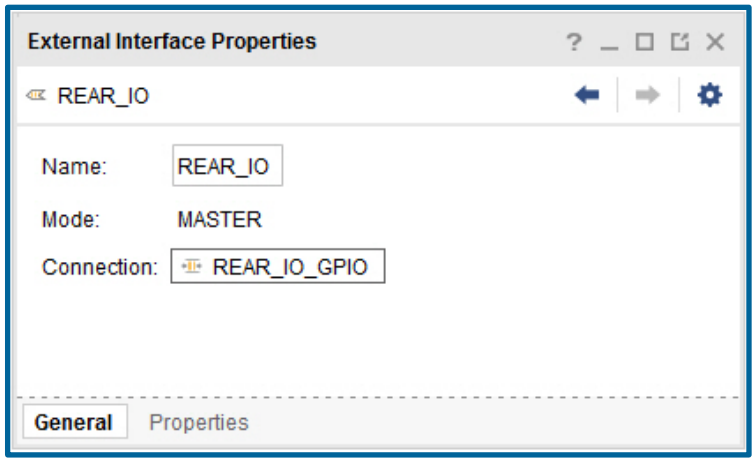
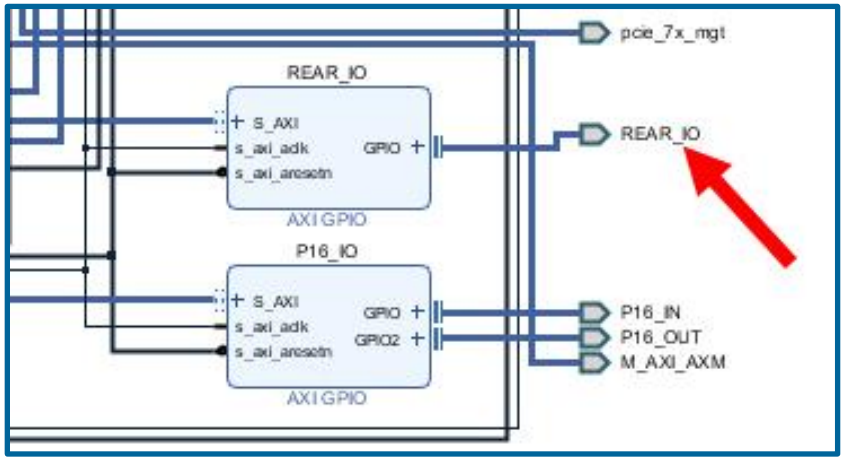


Figure 10



XMC-7A200 Design Modification Walk Through

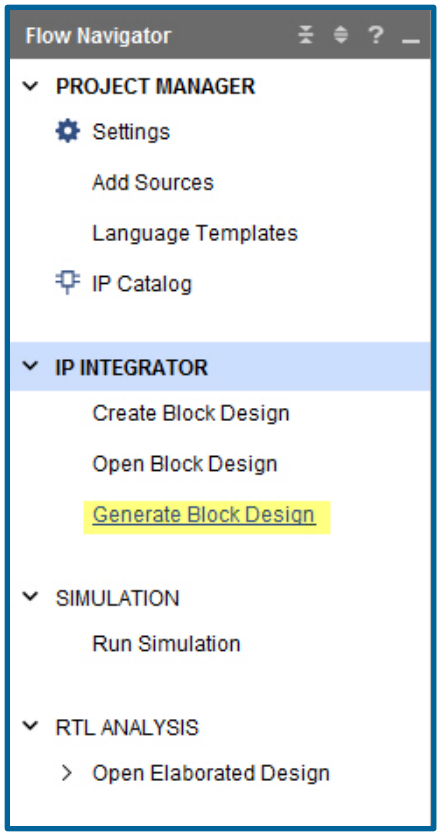


Figure 11

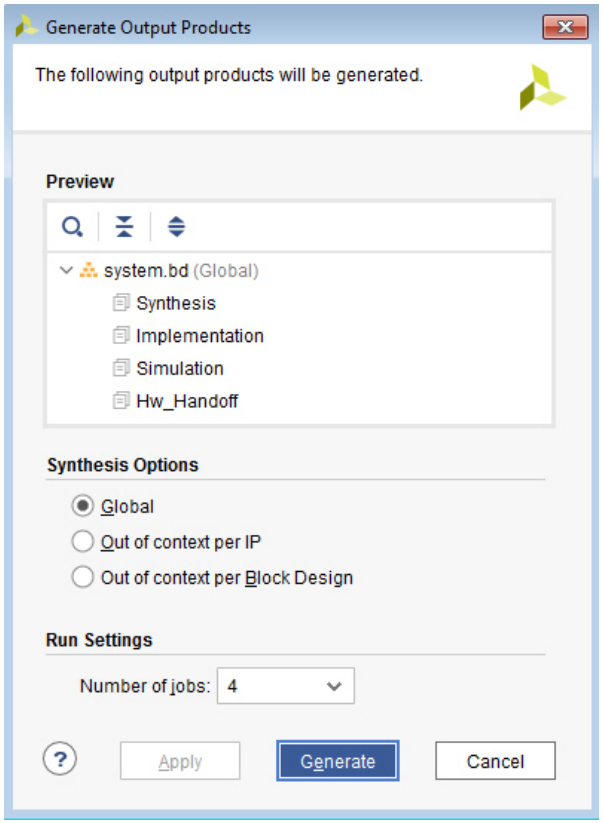


Figure 12

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XMC-7A200 Design Modification Walk Through

C:\XMC-7A200_MOD\XMC-7A200AX.xpr\XMC-7A200\XMC-7A200.srcs\sources_1\bd\system\hdl\system_wrapper.vhd

C:\XMC-7A200_MOD\XMC-7A200AX.xpr\XMC-7A200\XMC-7A200.srcs\sources_1\imports\system_top.vhd

Figure 13

```
187     M_AXI_AXM_rvalid : in STD_LOGIC;
188     M_AXI_AXM_wdata : out STD_LOGIC_VECTOR ( 31 downto 0 );
189     M_AXI_AXM_wready : in STD_LOGIC;
190     M_AXI_AXM_wstrb : out STD_LOGIC_VECTOR ( 3 downto 0 );
191     M_AXI_AXM_wvalid : out STD_LOGIC;
192     P16_IN_tri_i : in STD_LOGIC_VECTOR ( 15 downto 0 );
193     P16_OUT_tri_o : out STD_LOGIC_VECTOR ( 15 downto 0 );
194     PCI_RESETn : in STD_LOGIC;
195     PCIe_REFCLK : in STD_LOGIC;
196     REAR_IN_tri_i : in STD_LOGIC_VECTOR ( 31 downto 0 );
197     REAR_OUT_tri_o : out STD_LOGIC_VECTOR ( 31 downto 0 );
198     SYS_CLK_I : in STD_LOGIC;
199     S_AXI_ACLK : out STD_LOGIC;
200     S_AXI_ARESETN : out STD_LOGIC_VECTOR ( 0 to 0 );
201     Vp_Vn_v_n : in STD_LOGIC;
202     Vp_Vn_v_p : in STD_LOGIC;
203     mem_dq_i : in STD_LOGIC_VECTOR ( 15 downto 0 );
```

```
192     P16_IN_tri_i : in STD_LOGIC_VECTOR ( 15 downto 0 );
193     P16_OUT_tri_o : out STD_LOGIC_VECTOR ( 15 downto 0 );
194     PCI_RESETn : in STD_LOGIC;
195     PCIe_REFCLK : in STD_LOGIC;
196     REAR_IO_tri_i : in STD_LOGIC_VECTOR ( 31 downto 0 );
197     REAR_IO_tri_o : out STD_LOGIC_VECTOR ( 31 downto 0 );
198     REAR_IO_tri_t : out STD_LOGIC_VECTOR ( 31 downto 0 )
199     SYS_CLK_I : in STD_LOGIC;
```

Figure 14

XMC-7A200 Design Modification Walk Through

C:\XMC-7A200_MOD\XMC-7A200AX.xpr\XMC-7A200\XMC-7A200.srcs\sources_1\imports\system_top.vhd

```
129     CTRL27                      : inout STD_LOGIC;
130     CTRL28                      : inout STD_LOGIC;
131
132     -- The following signals are used to interface to the Rear I/O LVDS port
133     RI: in std_logic_vector (31 downto 0);
134     RO: out std_logic_vector (31 downto 0);
135
```

Figure 15

```
129     CTRL27                      : inout STD_LOGIC;
130     CTRL28                      : inout STD_LOGIC;
131
132     -- The following signals are used to interface to the Rear I/O LVDS port
133     RIO_P: inout std_logic_vector (31 downto 0);
134     RIO_N: inout std_logic_vector (31 downto 0);
135
```

Figure 16

```
293   signal AXM_INTERRUPT :  STD_LOGIC;
294   signal FLASH_addr_i : STD_LOGIC_VECTOR(24 downto 0);
295
296   signal REAR_IO_tri_i : STD_LOGIC_VECTOR ( 31 downto 0 );
297   signal REAR_IO_tri_o : STD_LOGIC_VECTOR ( 31 downto 0 );
298   signal REAR_IO_tri_t : STD_LOGIC_VECTOR ( 31 downto 0 );
299
```

Figure 17

XMC-7A200 Design Modification Walk Through

```
480     p16_in_tri_i => P16_SI,
481     p16_out_tri_o => P16_SO,
482     rear_in_tri_i => RI,
483     rear_out_tri_o => RO,
484     Vp_Vn_v_n => Vp_Vn_v_n,
485     Vp_Vn_v_p => Vp_Vn_v_p
486 );
```

Figure 18

```
480     p16_in_tri_i => P16_SI,
481     p16_out_tri_o => P16_SO,
482     REAR_IO_tri_i => rear_io_tri_i,
483     REAR_IO_tri_o => rear_io_tri_o,
484     REAR_IO_tri_t => rear_io_tri_t,
485     Vp_Vn_v_n => Vp_Vn_v_n,
486     Vp_Vn_v_p => Vp_Vn_v_p
```

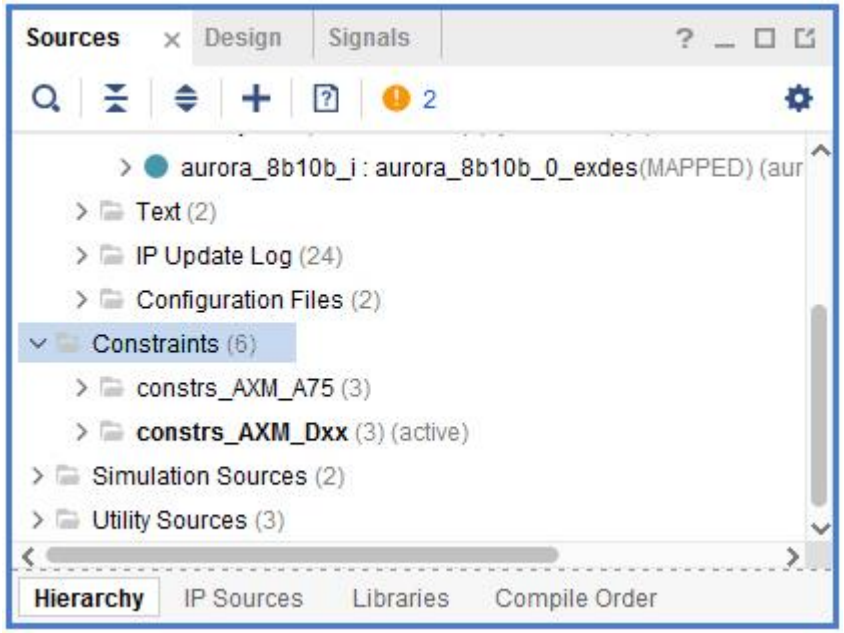
Figure 19

C:/XMC-7A200_2019p2/XMC-7A200_MOD/XMC-7A200AX.xpr/XMC-7A200/XMC-7A200.srcs/sources_1/imports/system_top.vhd

```
488
489 REAR_IO_IOB:    for i in 0 to 31 generate
490     begin
491             IOBUFDS_inst : IOBUFDS
492         generic map (
493             DIFF_TERM => FALSE,       -- Differential Termination (TRUE/FALSE)
494             IBUF_LOW_PWR => TRUE,     -- Low Power - TRUE, High Performance = FALSE
495             IOSTANDARD => "LVDS_25", -- Specify the I/O standard
496             SLEW => "SLOW")           -- Specify the output slew rate
497         port map (
498             O => rear_io_tri_i(i),    -- Buffer output
499             IO => RIO_P(i),           -- Diff_p inout (connect directly to top-level port)
500             IOB => RIO_N(i),          -- Diff_n inout (connect directly to top-level port)
501             I => rear_io_tri_o(i),    -- Buffer input
502             T => rear_io_tri_t(i)     -- 3-state enable input, high=input, low=output
503         );
504     end generate;
505
```

Figure 20

XMC-7A200 Design Modification Walk Through



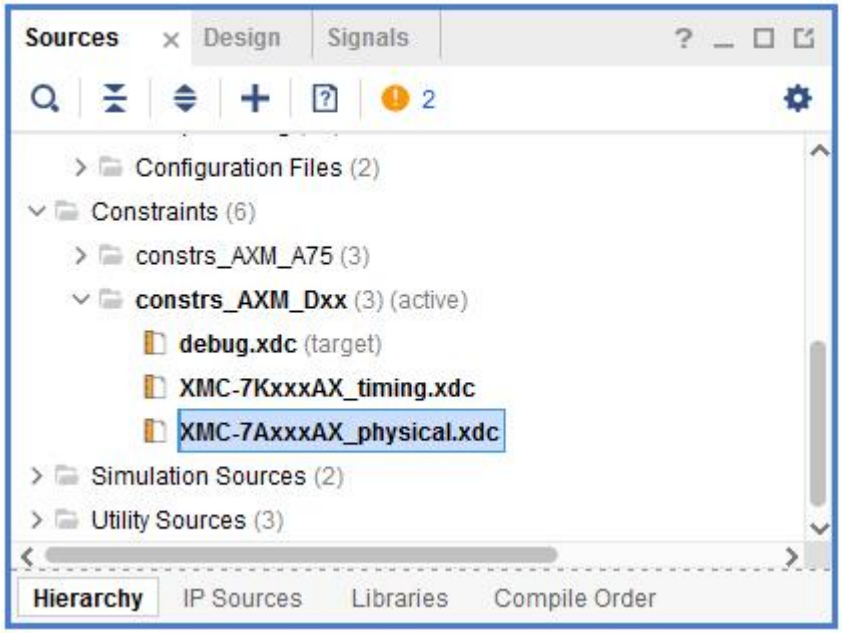


Figure 21

XMC-7A200 Design Modification Walk Through

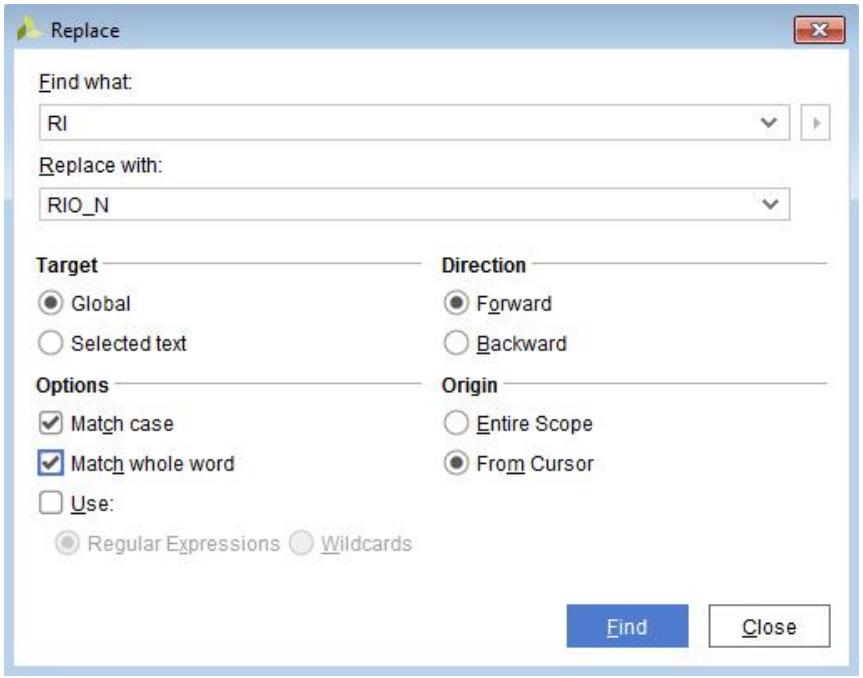
Diagram | Address Editor | system_wrapper.vhd | system_top.vhd | XMC-7AxxxAX_physical.xdc

C:/XMC-7A200_2019p2/XMC-7A200_MOD/XMC-7A200AX.xpr/XMC-7A200/XMC-7A200.srcs/constrs_AXM_Dxx/imports/XMC-7AxxxAX_physical.xdc

```
191 set_property PACKAGE_PIN H28 [get_ports {RI[0]}]
192 set_property PACKAGE_PIN J28 [get_ports {RO[0]}]
193 set_property PACKAGE_PIN H24 [get_ports {RI[1]}]
194 set_property PACKAGE_PIN J24 [get_ports {RO[1]}]
195 set_property PACKAGE_PIN G27 [get_ports {RI[2]}]
196 set_property PACKAGE_PIN H27 [get_ports {RO[2]}]
197 set_property PACKAGE_PIN J8 [get_ports {RI[3]}]
198 set_property PACKAGE_PIN J9 [get_ports {RO[3]}]
199 set_property PACKAGE_PIN G26 [get_ports {RI[4]}]
200 set_property PACKAGE_PIN H26 [get_ports {RO[4]}]
201 set_property PACKAGE_PIN G34 [get_ports {RI[5]}]
202 set_property PACKAGE_PIN H33 [get_ports {RO[5]}]
203 set_property PACKAGE_PIN G25 [get_ports {RI[6]}]
204 set_property PACKAGE_PIN G24 [get_ports {RO[6]}]
205 set_property PACKAGE_PIN K32 [get_ports {RI[7]}]
206 set_property PACKAGE_PIN L32 [get_ports {RO[7]}]
207 set_property PACKAGE_PIN G30 [get_ports {RI[8]}]
208 set_property PACKAGE_PIN G29 [get_ports {RO[8]}]
209 set_property PACKAGE_PIN L30 [get_ports {RI[9]}]
210 set_property PACKAGE_PIN L29 [get_ports {RO[9]}]
211 set_property PACKAGE_PIN L24 [get_ports {RI[10]}]
212 set_property PACKAGE_PIN M24 [get_ports {RO[10]}]
213 set_property PACKAGE_PIN J30 [get_ports {RI[11]}]
214 set_property PACKAGE_PIN K30 [get_ports {RO[11]}]
215 set_property PACKAGE_PIN L25 [get_ports {RI[12]}]
216 set_property PACKAGE_PIN M25 [get_ports {RO[12]}]
217 set_property PACKAGE_PIN G31 [get_ports {RI[13]}]
```

Figure 22

XMC-7A200 Design Modification Walk Through



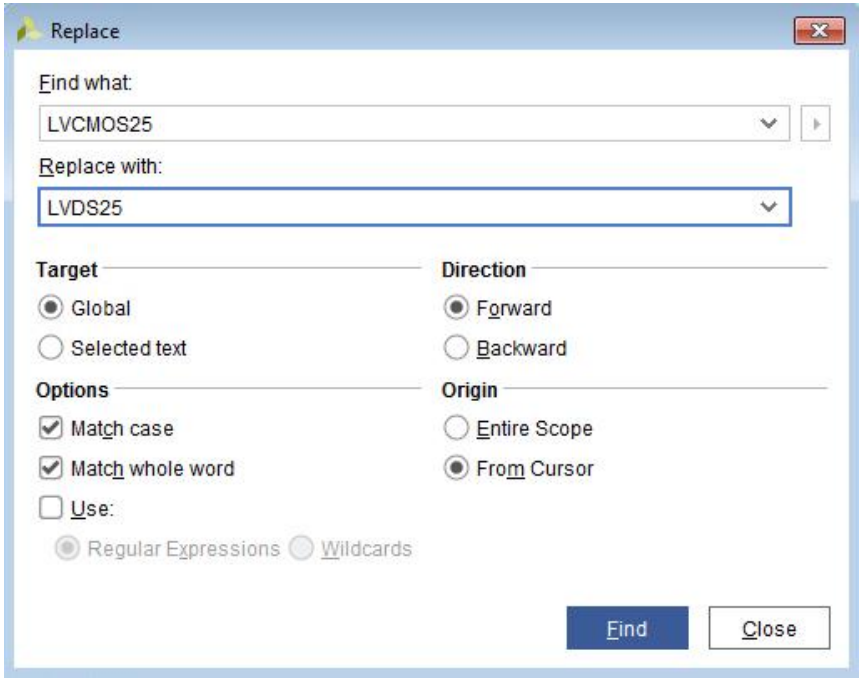


Figure 23

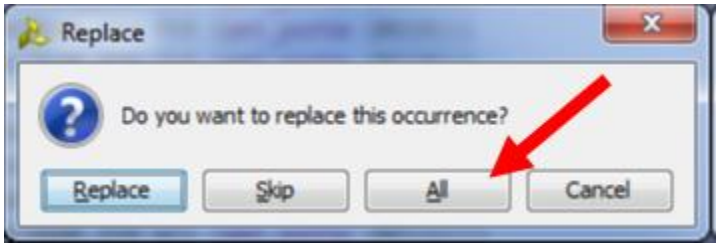


Figure 24

XMC-7A200 Design Modification Walk Through

C:/XMC-7A200_2019p2/XMC-7A200_MOD/XMC-7A200AX.xpr/XMC-7A200/XMC-7A200.srcs/constrs_AXM_Dxx/imports/XMC-7AxxxAX_physical.xdc

```
190
191 set_property PACKAGE_PIN H28 [get_ports {RIO_N[0]}]
192 set_property PACKAGE_PIN J28 [get_ports {RO[0]
193 set_property PACKAGE_PIN H24 [get_ports {RIO_N[1]}]
194 set_property PACKAGE_PIN J24 [get_ports {RO[1]}]
195 set_property PACKAGE_PIN G27 [get_ports {RIO_N[2]}]
```

"64" occurrences have been replaced

Figure 25: “RI” to “RIO_N”

C:/XMC-7A200_2019p2/XMC-7A200_MOD/XMC-7A200AX.xpr/XMC-7A200/XMC-7A200.srcs/constrs_AXM_Dxx/imports/XMC-7AxxxAX_physical.xdc

```
190
191 set_property PACKAGE_PIN H28 [get_ports {RIO_N[0]}]
192 set_property PACKAGE_PIN J28 [get_ports {RIO_P[0]}]
193 set_property PACKAGE_PIN H24 [get_ports {RIO_N
194 set_property PACKAGE_PIN J24 [get_ports {RIO_P[1]}]
195 set_property PACKAGE_PIN G27 [get_ports {RIO_N[2]}]
```

"64" occurrences have been replaced

Figure 26: “RO” to “RIO_P”

C:/XMC-7A200_2019p2/XMC-7A200_MOD/XMC-7A200AX.xpr/XMC-7A200/XMC-7A200.srcs/constrs_AXM_Dxx/imports/XMC-7AxxxAX_physical.xdc

```
256
257 set_property IOSTANDARD LVDS25 [get_ports {RIO_N[31]}]
258 set_property IOSTANDARD LVDS25
259 set_property IOSTANDARD LVDS25 [get_ports {RIO_N[29]}]
260 set_property IOSTANDARD LVDS25 [get_ports {RIO_N[28]}]
261 set_property IOSTANDARD LVDS25 [get_ports {RIO_N[27]}]
```

"64" occurrences have been replaced

Figure 27: “LVCMOS25” to “LVDS25”

XMC-7A200 Design Modification Walk Through

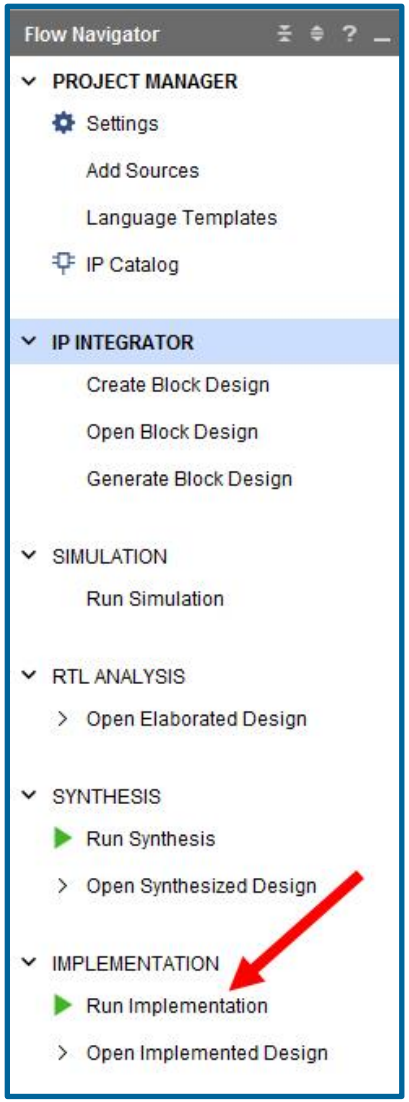


Figure 28

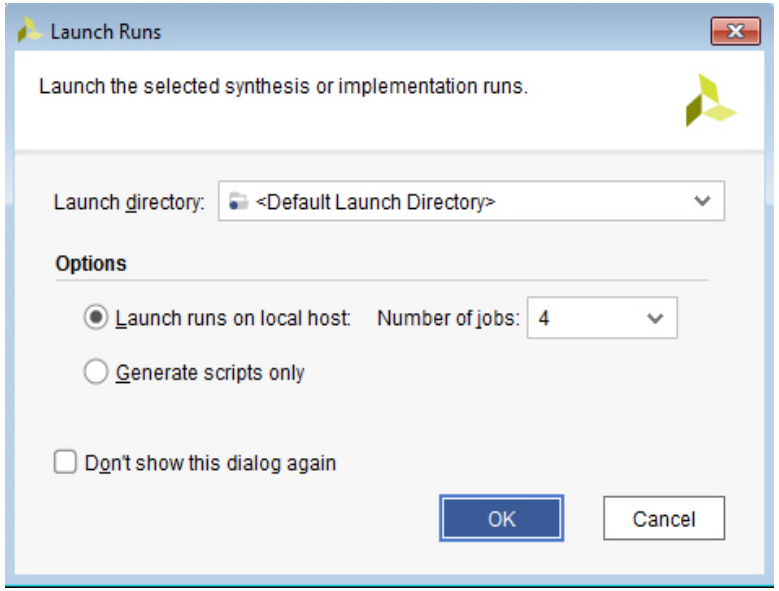
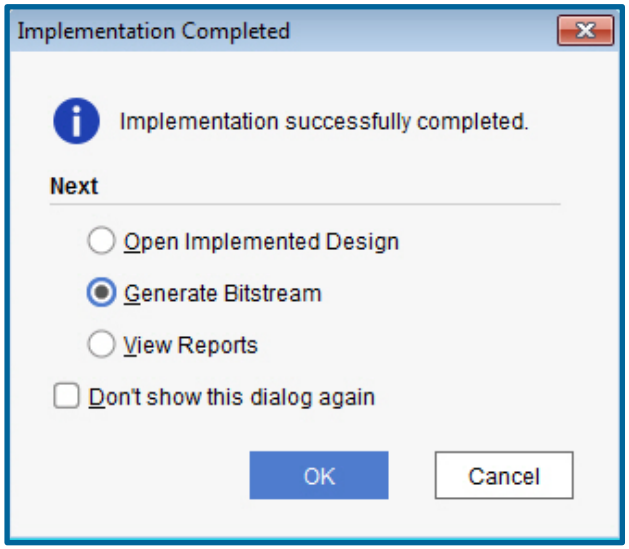


Figure 29

Figure 30



XMC-7A200 Design Modification Walk Through

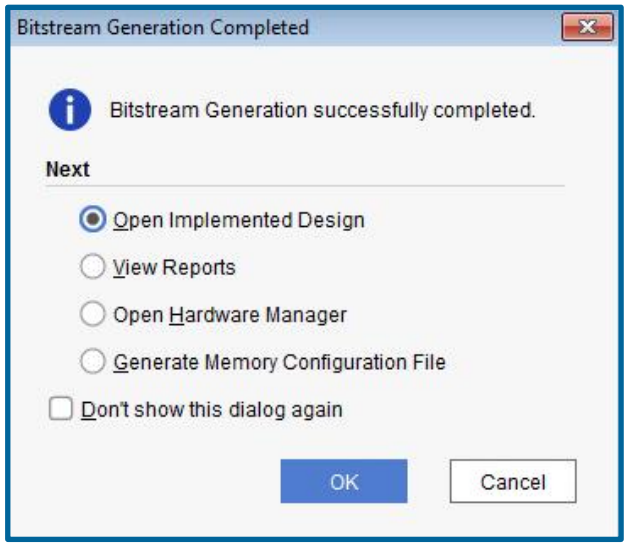
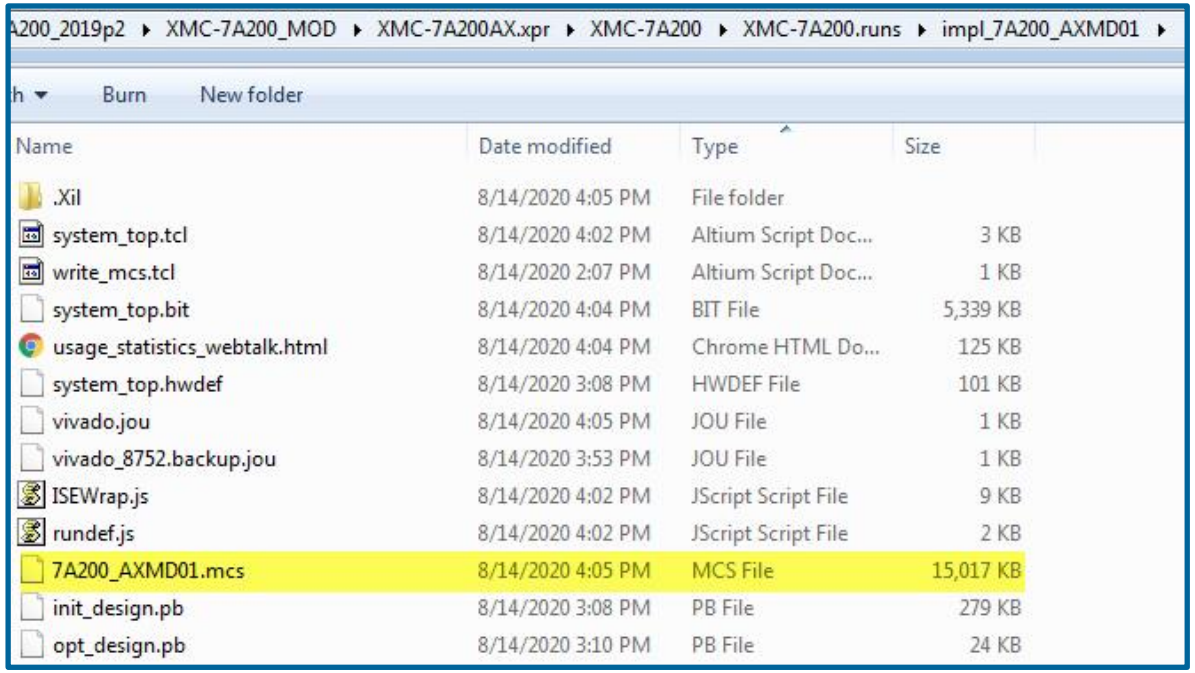


Figure 31

Figure 32



C:\XMC-7A200_MOD\XMC-7A200AX.xpr\XMC-7A200\XMC-7A200.runs\impl_7A200_AXMD01\7A200_AXMD01.mcs

Future Topics Part 3 of 3

- Acropack Zync Ultrascale
- Features of APZU
- Advantages of Zync Ultrascale

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The End

THANK YOU.